A Gate Drive Circuit With Mid-Level Voltage for GaN Transistors in A 7-MHz Isolated Resonant Converter*

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***Abstract*-This paper analyzes the drive requirements of Gallium Nitride (GaN) power transistors as the control FETs in the resonant converters in the range of multi-megahertz. In resonant converters with multi-MHz, ZVS technique is normally used to reduce the high frequency switching loss. The commercial gate drivers for the GaN transistors focus on high reliability to the precise gate drive voltage against the parasitic components. But they do not consider the high reverse conduct voltage of the GaN transistors as the control FETs under ZVS at high frequency. To reduce the high reverse conduction loss of the GaN power transistors due to the reverse conduction mechanism before ZVS turn-on, in the meanwhile, ensure the high stability and reliability, a new driving scheme with the mid-level voltage is proposed. In addition, the proposed drive circuit is applied to an isolated resonant DC-DC converter with 7 MHz. The prototype of 18 V input and 5 V/ 2 A output was built to verify the functionality and the benefits.**

***Keywords*-GaN transistor; gate driver; resonant converter; ZVS**

I. INTRODUCTION

With excellent Figure of Merit (FOM), Gallium Nitride (GaN) power transistors are expected to drive the power converters to higher frequency, higher power density and higher efficiency. The lateral structure of the GaN transistors makes it a very low charge device. They can switch hundreds of volts in nanoseconds, giving them multiple megahertz capability [1-4]. However, the GaN transistors could not replace Silicon MOSFETs in the power circuit straightway. Some intrinsic characteristics make the considerations must be taken when the GaN transistors are used. To begin with, the gate-to-source voltage requirement is stringent, that it cannot exceed the 6V maximum rating. Then, the care should be taken to prevent false turn on of the switches on account of the low threshold voltage V_{th}. Finally, there is no body-diode, so the reverse current has to flow via the channel by the reverse conduction mechanism, causing high reverse conduction loss.

Some research has been done on the drive design of the GaN transistors. A three-level driving method is proposed to reduce the reverse conduction loss of the Synchronous Rectifier (SR) in a synchronous Buck converter in [5]. However, the driving method is limited to the GaN FETs as SRs. The negative bias of 2 V from the gate to the source is added to prevent the false turn-on of the switches in [6]. However, the negative bias also increases the risk of exceeding the -5 V minimum rating of the gate-to-source voltage. Moreover for the GaN transistors realizing ZVS turn-on, the reverse conduct voltage is increased, which results in high reverse conduction loss by the negative bias voltage from the gate to the source because of the reverse conduction mechanism. As the switching frequency increases, the reverse conduction loss before ZVS turn-on becomes severe and cannot be neglected. Therefore, how to decrease the reverse conduction loss before ZVS turn-on of the control FET in the resonant converters and at the same time, ensure the high reliability and stability remain to be investigated.

The objective of this paper is to explore the driving scheme to drive the GaN power transistors especially as the control FETs in the resonant converters in the frequency range of multi-megahertz to realize high reliability and efficiency. The benefits of the proposed driving scheme are summarized as follows: 1) excellent *dv/dt* immunity; 2) reduced gate-to-source voltage oscillation during the switching transition; 3) lower reverse conduction loss of the GaN transistors under ZVS turn-on condition.

II. CHALLENGES OF DRIVING REQUIREMENTS FOR GAN TRANSISTORS IN THE RANGE OF MULTI-MEGAHERTZ

Due to the intrinsic characteristics of the GaN power transistors, careful design considerations have been taken for the gate drivers especially at high switching frequency in the range of multi-megahertz. Two important design points need special attention and are analyzed in detail, including 1) false turn-on problem; and 2) high reverse conduction loss before ZVS turn-on.

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A. False Turn-on Caused by the Under-damped Discharge Loop

Fig. 1 shows the conventional gate drive structure of a Si MOSFET. R_g is the gate drive resistor, which allows adjustment of the MOSFET turn-on speed and the anti-parallel diode D_g is used to accelerate the speed of turn-off. However, for the GaN transistor, the threshold voltage V_{th} is as low as 1.4V typically, and D_g has the forward drop of 0.7 V, which reduces the effective gate discharge current when the gate-to-source voltage approaches 0 V, therefore D_g must be avoided. So the gate structure in Fig. 2 is normally recommended to drive the GaN transistors because it has the separate sink and source outputs to make it excellent for fast turn off and *dv/dt* immunity, in the meanwhile avoid overshoot on the gate that may exceed the absolute maximum rating by picking the appropriate R_g [7].

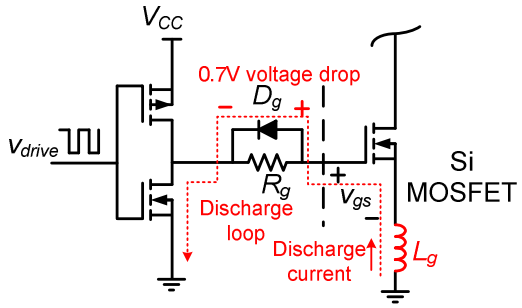


Fig. 1 Conventional gate drive structure of Si MOSFETs

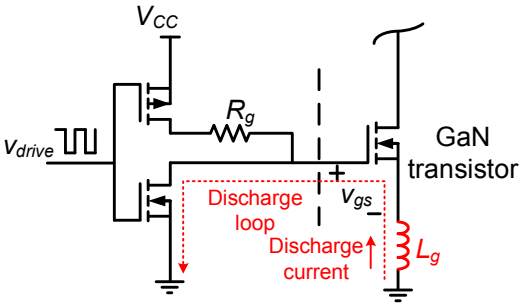


Fig. 2 Gate Drive Structure of GaN Power Transistors

L_g is the common source inductance of the switch, which is defined as the inductance shared by the power stage and driver loop in Fig. 1 and Fig. 2. To ensure fast turn off and excellent *dv/dt* immunity of the GaN power transistor, the damping of the discharge loop must be minimized. However, it is found that severe oscillation of the gate-to-source voltage appears in the under-damped loop caused by the L_g when the GaN transistor turns off in the frequency range of multi-megahertz. The oscillation amplitude could be higher than the threshold voltage of the GaN transistor, which causes false turn-on of the switch.

Fig. 3 shows the simulation waveform of the gate-to-source voltage using the drive circuit in Fig. 2 when the switching frequency is 7 MHz and the gate inductance L_g is 3 nH. The pull-up resistance of totem pole is 2 Ω and the pull-down resistance is 0.24 Ω, which is the same as the drive IC LM5114. It can be observed that the oscillation amplitude is 1.2 V, approaching the typical threshold voltage V_{th} of the GaN transistor and may cause false turn-on.

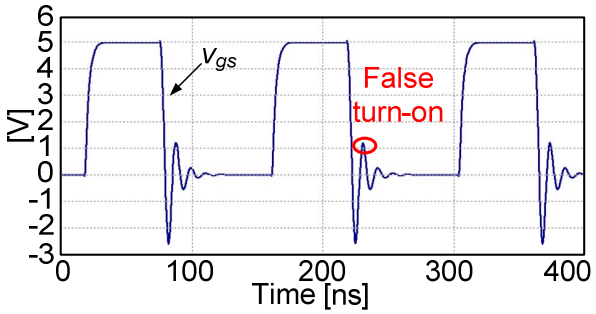


Fig. 3 False turn-on caused by the oscillation

More importantly, with the gate inductance increasing and the crosstalk by other loop, the oscillation will be more severe and the amplitude can exceed V_{th} easily, causing the false turn-on of the switches. Furthermore, *dv/dt* from the drain to the source after the turn-off of the switch via the miller capacitance inducing a positive voltage from the gate to the source will increase the risk of false turn-on of the switch by superposition theorem.

To solve the problem above, an appropriate negative voltage from the gate to the source is added to increase the margin of the oscillation amplitude and prevent false turn-on of the switches in [6]. With the negative bias from the gate to the source, the *dv/dt* immunity is improved and it is unnecessary to minimize the damping resistance of the discharge circuit and thus the gate voltage oscillation can be damped more strongly. So, different from the driver in [6], a resistor is preferred to be connected in series in the discharge loop to reduce the oscillation, which results in extra power loss and the risk of exceeding the -5 V minimum rating of the gate-to-source voltage.

B. Reverse Conduction Loss before ZVS Turn-on

In addition to the problem of preventing false turn-on of the switch mentioned above, another important point is the reverse conduction loss before ZVS turn-on.

The reverse conduction mechanism of the SR has been analyzed in [5]. However, there is no reported analysis considering the GaN transistors as the control FET under ZVS condition. In the frequency range of multi-megahertz, the switch normally operates under ZVS condition to reduce the high frequency switching loss. The reverse current needs to flow through the switch before the ZVS turn-on, which will trigger the reverse conduction mechanism.

Fig.4 shows the equivalent model for the GaN power transistors. To achieve ZVS turn-on, as control FETs in the resonant converters, before gate signal building up, v_{gs} unchanged. When current flows into the source terminal, it will charge C_{GD} and C_{DS}. Till the capacitor voltage v_{gd} is approaching the threshold voltage V_{th}, the channel begins to build up. Then the current will flow via the channel, that's the reverse conduction mechanism.

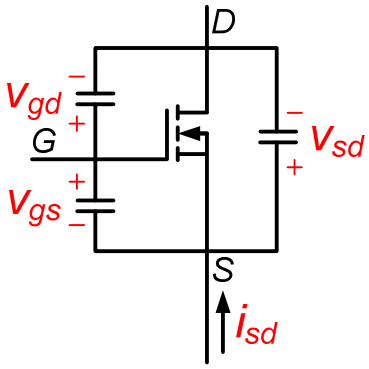


Fig. 4 GaN transistor with parasitics as the control FET under ZVS

As shown in Fig. 4, the voltage drop across the source to the drain is

$$v_{sd} = v_{gd} - v_{gs} \tag{1}$$

Fig. 5 gives the relationship between V_{GS}, V_{DS} and I_{DS}. From Fig. 5, it can be observed that The reserve voltage drop is 2 V with V_{GS}=2 V. This is much higher the forward voltage of the body diode of a Si MOSFET. Furthermore, the reverse conduct voltage decreases with the gate-to-source voltage increases.

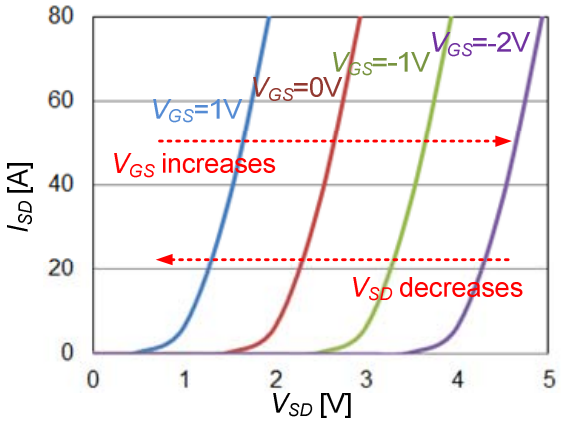


Fig. 5 V_{SD}-I_{SD} curve of the GaN Power Transistor(EPC2001)

With the negative bias of -2 V added from the gate to the source when the transistor is turned off, the reverse conduct voltage can be larger than V_{th}-(-2 V), which is shown in Fig. 5. Importantly, when the switching frequency increases to a level that the reverse conduction time is no longer negligible and the reverse conduct voltage is much higher than that of a Si MOSFET, the reverse conduction period before the ZVS turn-on of the control FET causes high conduction loss due to the GaN reverse conduction mechanism.

The reverse conduction loss P_R before ZVS turn-on can be expressed as:

$$P_R = V_{SD} \cdot I_{SD} \cdot t_r \cdot f_s \tag{2}$$

where V_{SD} is the voltage drop, I_{SD} is the reverse conduct current, t_r is the reverse conduction time and f_s is the switching frequency. To reduce the reverse conduction loss in the switching frequency range of multi-megahertz, we could minimize V_{SD}, I_{SD} or t_r as low as possible.

Actually, I_{SD} relies on the converter specifications. The reverse conduction time t_r is related to the load condition of the resonant converter, so in the practical circuit design, t_r should consider the worst condition to allow the drain current to discharge the output capacitance of the transistor so that ZVS turn-on of the switch can guaranteed. So the practical method of decreasing V_{SD} is useful to reduce the reverse conduction loss by using a positive bias V_x (V_x<V_{th}) from the gate to the source to replace the negative bias before the ZVS turn-on of the switch. As shown in Fig. 5, the reverse conduct voltage and reverse conduct loss decreases with the gate-to-source voltage increases.

As a conclusion, to decrease the reverse conduct voltage, it is effective to add a positive bias from the gate to source before the GaN transistor turned on. The point is the positive bias amplitude has to be lower than threshold voltage to avoid the short through issue.

III. Proposed Gate Drive Circuit for GaN Transistors

Based on the above analysis of the driving requirements of the GaN transistor as the control FET, the basic idea is to use a positive bias added across the gate-to-source before the ZVS turn-on to decrease the reverse conduction loss, meanwhile use a negative bias after the turn off transition to ensure the high reliability. So Fig. 6 illustrates the preferred drive voltage waveform.

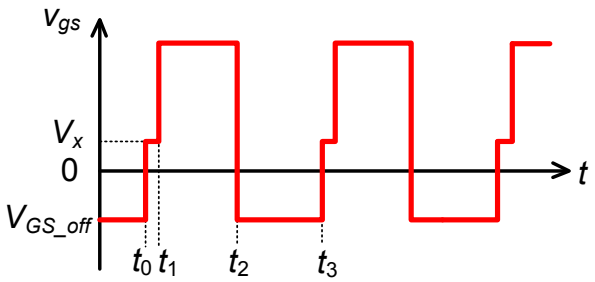


Fig.6 Constructed drive voltage waveform for the GaN transistor as the control FET

Fig. 7 shows the schematic of the proposed driving scheme. With the schematic, the drive waveform in Fig.5 can be realized. The mid-level generator provides the positive bias from t_0 to t_1. D_z is a Zener diode to provide the negative voltage from the gate to the source and R_z is a resistor adjusting the current flow into Zener diode to ensure the reverse conduction of the Zener diode. C_1 and C_2 are filter capacitors.R_{g1} and R_{g2} are used to adjust the damping of charge and discharge loop of the input capacitor of the GaN power transistor separately. OSC and CON are 60% duty cycle square wave signals, and CON is ahead of OSC. The phase shift is determined by the reverse conduction time t_r to guarantee the ZVS turn-on of the switch in the worst condition.

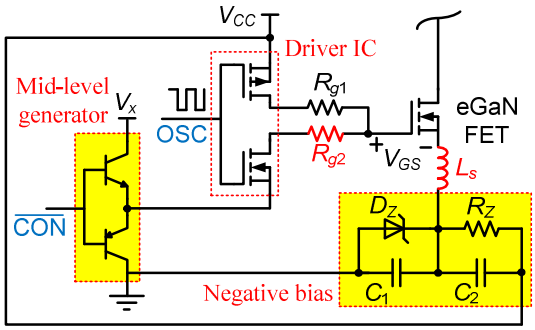


Fig.7 Proposed driving scheme

From Fig. 6, the switching intervals are analyzed as follows:

1) Stage 1 *[t_0, t_1]*

The control FET is ready to realize ZVS turn-on, and the reverse current flows into source, causing the reverse conduction mechanism triggered.

A positive bias V_x is added from the gate to source, making the reverse conduct voltage decrease from V_{th} to V_{th}-V_x. The duration of this stage should be decided to ensure ZVS turn-on under different load. This stage ends at $t = t_1$ when the control FET turns on.

2) Stage 2 *[t_1, t_2]*

During this stage, control FET is turned on softly. With an appropriate resistor to make up an over-damped circuit to charge the input capacitor of the GaN transistor, there's no oscillation of the gate-to-source voltage, which prevents the voltage exceeding the maximum rating.

The switch is in the conduction state until the stage ends at $t = t_2$.

3) Stage 3 *[t_2, t_3]*

During this stage, control FET is turned off.

A negative bias is added from the gate to the source, making the switch excellent *dv/dt* immunity. An appropriate resistor is connected in series in the discharge loop to inhibit the oscillation.

This stage ends at $t = t_3$ when the control FET is going to reverse conduct.

Fig. 8 shows the simulation waveform of the proposed driving scheme. The R_{g1} is 0 Ω and the R_{g2} is 1 Ω. The gate inductance is 3 nH. The pull-up resistance of totem pole in the driver IC is 2 Ω and the pull-down resistance is 0.24 Ω in the simulation, which is the same as the driver LM5114. The simulation result agrees with the theoretical analysis and verifies the functionality of the proposed driving scheme.

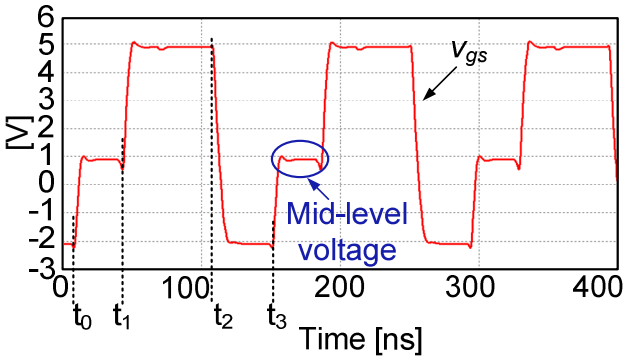


Fig.8 Simulation waveform of the proposed driving scheme

IV. Experimental Results and Discussion

To verify the functionality of the proposed driving scheme of the GaN power transistor, an isolated resonant converter with the applied driving scheme is implemented.

The specifications of the isolated resonant converter are shown in TABLE I. The topology of the isolated resonant DC-DC converter is shown in Fig. 9. The converter is composed of the Class-Φ_2 inverter and the Class-E rectifier [7-9]. The control FET S_m can realize ZVS in the topology.

TABLE I. Specifications of the Converter

Input voltage	18 V~36V
switching frequency	7 MHz
Output voltage	5 V
Output current	2 A

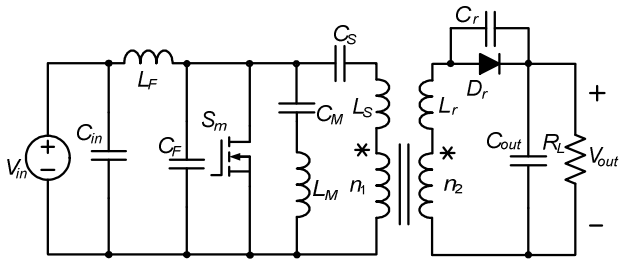
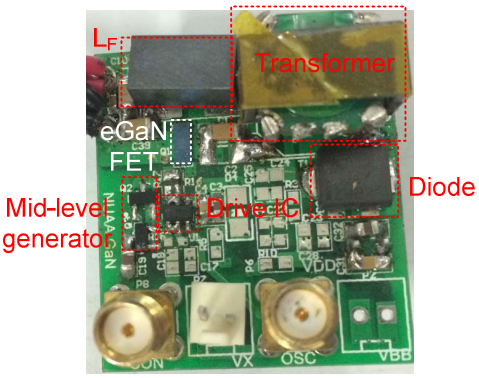


Fig.9 Isolated resonant DC-DC converter

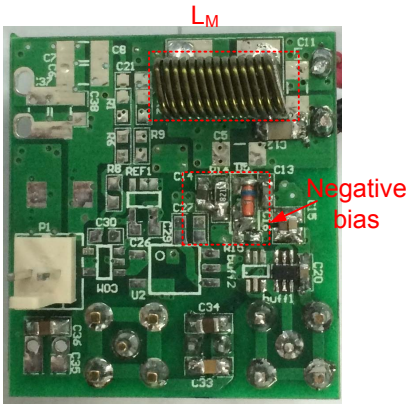
A 7 MHz, 18 V input, 10 W/ 5 V output isolated resonant DC-DC converter using the GaN power transistor EPC2001 from EPC is implemented. The parameters are given in TABLE II. The photo of the prototype is shown in Fig. 10. The driver IC is LM5114 and a Zener diode is applied to have -2 V from the gate to the source. The R_{g2} is replaced by the equivalent conduct resistor of NPN bipolar transistor in the mid-level generator.

TABLE II. Power Stage Component Values

L_F	300 nH	C_F	450 pF
L_M	300 nH	C_M	375 pF
C_S	8 nF	C_r	3 nF
C_{in}	20 µF	C_{out}	47 µF



(a) Top



(b)Bottom

Fig. 10 Photo of prototype

As a comparison to the proposed drive scheme, the gate-to-source and the drain-to-source voltage waveforms using the drive scheme without the midlevel generator are shown in Fig. 11. To ensure wide range operation of ZVS, the worst case has been considered in the resonant converter. A negative 2 V is added from the gate to source when the GaN power transistor is turned off, and the turn-off oscillation is inhibited by the R_{g2} of 1 Ω. As shown in Fig. 11, with the negative bias of 2 V added from the gate to source before the ZVS turn-on, the reverse conduct voltage is about –4 V. The gate-to-source and drain-to-source voltage waveforms using the drive scheme with the midlevel generator are shown in Fig. 12. With a positive voltage added from the gate to source before the ZVS turn-on of the transistor, the largest reverse conduct voltage is reduced to -2V. The reverse conduct voltage is reduced to half of that using the driver without the midlevel generator, so is the reverse conduction loss. The effect of reducing the reverse conduct voltage and reverse conduction loss by the proposed drive scheme is verified. It should be pointed the reverse condition time is 16 ns and this is worst case for ZVS achievement in this converter.

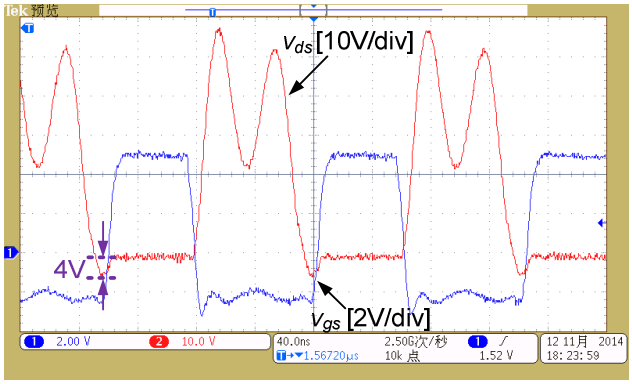


Fig. 11 Waveforms of v_{GS}, v_{DS}: without the midlevel generator

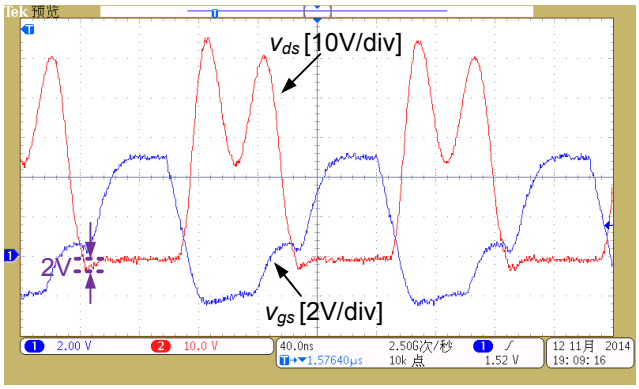


Fig. 12 Waveforms of v_{GS}, v_{DS}: with the midlevel generator

V. Conclusion

A driving scheme with the mid-level voltage for the GaN power transistors as the control FETs in the high frequency resonant DC-DC converters is proposed. The driving scheme can ensure the high stability and reliability of the transistor, in the meanwhile, decrease the high reverse conduction loss before ZVS turn-on. The simulation results verify the functionality of the proposed GaN driver. In addition, the proposed new driver is applied to an isolated resonant DC-DC converter with 7 MHz. The prototype of 18 V input and 5 V/ 2 A output was built to verify the new drive circuit and the benefits.

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